CA

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/576,246	09/27/2006	Henning Sirringhaus	Q94482	8834

23373 7590 05/31/2007

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
LEE, JAE	

ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
05/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/576,246	SIRRINGHAUS ET AL.	
	Examiner	Art Unit	
	Jae Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/17/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

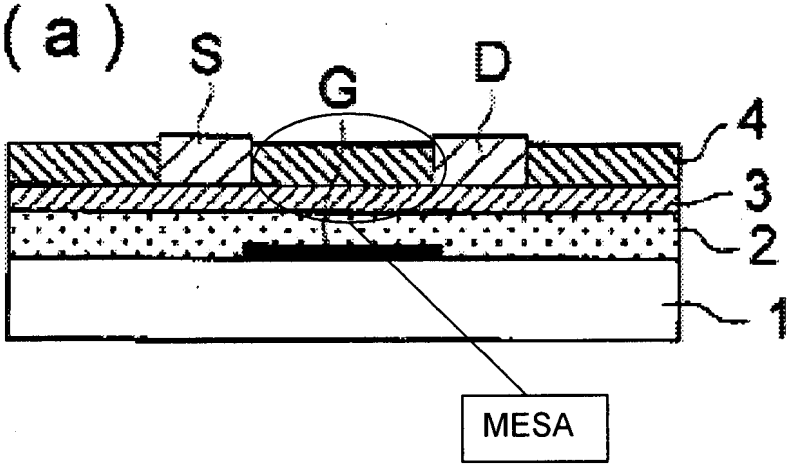
Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1,3-7,9-11,13,14,16,18,19,22-24,26,28-30** are rejected under 35 U.S.C. 102(e) as being anticipated by Hirai (Pub No. US 2003/0160235 A1, hereinafter Hirai et al.).

FIG. 1 (a)



With regards to **claim 1**, Hirai et al. teaches a thin film transistor electronic switching device, comprising:

a source electrode and a drain electrode (see Fig. 1a, source **S** and drain **D**);

a semiconducting region in contact with and extending between the source and drain electrodes (see Fig. 1a, organic semiconductor layer **3**);

a gate electrode disposed for influencing the transconductance of at least part of the semiconducting region (see Fig. 1a, gate electrode **G**, inherent that the gate electrode will influence transconductance since drain current and the gate electrode voltage will change during operation of the device, $g_m = dI / dE$, where dI = change in drain current and dE = change in gate voltage); and

an insulating region located between the source and drain electrodes and configured so that the length of the shortest current path through the semiconducting region between the source and drain electrodes is greater than the shortest physical distance between the source and drain electrodes (see Fig. 1a, insulating region **4**, current path between **S** and **D** must be larger than the physical separation distance between **S** and **D**).

With regards to **claim 3**, Hirai et al. teaches a device as claimed in **claim 1**, wherein the shortest current path through the semiconducting region lies closer to the gate electrode than to all paths of the shortest physical distance between the source and drain electrodes (see Fig. 1a, current path between **S** and **D** will be closer to the gate electrode than the physical distance between any point of **S** and any point of **D**).

With regards to **claim 4**, Hirai et al. teaches a device as claimed in **claim 1**, wherein the source and drain electrodes comprise an inorganic metallic conductor (see ¶77, lines 1-2).

With regards to **claim 5**, Hirai et al. teaches a device as claimed in **claim 1**, wherein the source and drain electrodes comprise a conducting polymer (see ¶77, lines 1-2).

With regards to **claim 6**, Hirai et al. teaches a device as claimed in **claim 1**, wherein the semiconducting region comprises a solution processible conjugated polymeric or oligomeric material (see ¶84).

With regards to **claim 7**, Hirai et al. teaches a device as claimed in **claim 1**, wherein the semiconducting region comprises a material of small conjugated molecules with solubilizing side chains (see ¶97, lines 1-3,28, functional groups utilized).

With regards to **claim 9**, Hirai et al. teaches a device as claimed in **claim 1**, wherein the semiconductor region comprises an inorganic semiconductor or nanowires (see ¶97, line 53).

With regards to **claim 10**, Hirai et al. teaches a device as claimed in **claim 1**, wherein the semiconductor region has a mobility exceeding 10^{-3} cm^2/V (see ¶129, line 4).

With regards to **claim 11**, Hirai et al. teaches a device as claimed in **claim 1**, wherein the source and drain electrodes make ohmic contact with the semiconducting region (see Fig. 1a, semiconducting region **3** in contact with source **S** and drain **D**).

With regards to **claim 13**, Hirai et al. teaches a device as claimed in **claim 1**, wherein the device has a layer that comprises the source and drain electrodes and a layer that comprises the semiconductor region (see Fig. 1a, semiconductor region **3** is one layer, electrodes produced by lift-off procedure, see ¶77, lines 1-4).

With regards to **claim 14**, Hirai et al. teaches a device as claimed in **claim 1**, wherein said insulating region comprises a mesa structure of a dielectric material (see Fig. 1a, mesa formed).

With regards to **claim 16**, Hirai et al. teaches a device as claimed in **claim 1**, comprising a gate dielectric layer between the gate electrode and the semiconducting region (see Fig. 1a, gate dielectric layer **2**).

With regards to **claim 18**, Hirai et al. teaches a method for forming a thin film transistor electronic switching device, the method comprising:

forming a source electrode and a drain electrode (see Fig. 1a, source **S** and drain **D**);

forming a semiconducting region in contact with and extending between the source and drain electrodes (see Fig. 1a, organic semiconductor layer **3**);

forming a gate electrode disposed for influencing the transconductance of at least part of the semiconducting region (see Fig. 1a, gate electrode **G**, intended use limitations have no patentable significance); and

forming an insulating region located between the source and drain electrodes and configured so that the length of the shortest current path through the semiconducting region between the source and drain electrodes exceeds the shortest physical distance between the source and drain electrodes (see Fig. 1a, insulating region **4**, current path between **S** and **D** must be larger than the physical separation distance between **S** and **D**).

With regards to **claim 19**, Hirai et al. teaches a method as claimed in **claim 18**, wherein the step of forming the semiconducting region is performed after the step of forming the insulating region, the semiconducting region is deposited from solution in contact with the insulating region and the insulating region is capable of repelling the solution from which the semiconducting region is deposited (see Fig. 4a, semiconducting region **3** formed after insulating region **4** formed; ¶55, lines 5-13,

hydrophilic coating on surface will have capability to repel hydrophobic semiconducting region, e.g. organic).

With regards to **claim 22**, Hirai et al. teaches a method as claimed in **claim 18**, wherein the source and drain electrodes are formed by inkjet printing (see ¶76, lines 4-13).

With regards to **claim 23**, Hirai et al. teaches a method as claimed in **claim 18**, wherein the source and drain electrodes are formed by a continuous film coating technique (see ¶77, lines 1-4, lift-off method is continuous film coating technique).

With regards to **claim 24**, Hirai et al. teaches a method as claimed in **claim 18**, wherein one or more components of the device are deposited by vacuum deposition and patterned by photolithography (see ¶48, gate electrode formed by vacuum evaporation).

With regards to **claim 26**, Hirai et al. teaches a method as claimed in **claim 18**, wherein said insulating region is defined by a lithographic patterning technique (see Fig. 1a, insulating region 4 with through holes etched).

With regards to **claim 28**, Hirai et al. teaches a method as claimed in **claim 18**, wherein said insulating region is formed by depositing an insulating material onto the

substrate, wherein the insulating material preferably deposits in the region between the source and drain electrodes, but not on top of the source-drain electrodes (see Fig. 1a, insulating region **4** between source **S** and drain **D** and not on top of the electrodes).

With regards to **claim 29**, Hirai et al. teaches a method as claimed in **claim 28**, wherein said insulating material is deposited from a liquid phase (see ¶55, lines 1-4).

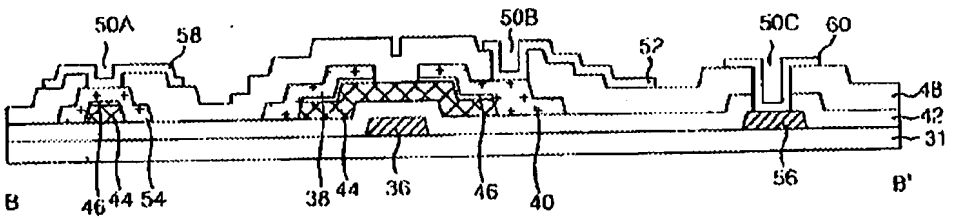
With regards to **claim 30**, Hirai et al. teaches a method as claimed in **claim 28**, wherein said insulating material is deposited form a vapor phase (see ¶50, lines 7-8, ¶55, lines 1-2, insulating region **4** can be produced using CVD).

3. **Claim 8** is rejected under 35 U.S.C. 102(e) as being anticipated by Hirai et al. as evidenced by Konstantinos et al. (Japanese Pub No. 2000-260999, hereinafter Konstantinos et al.).

With regards to **claim 8**, Hirai et al. teaches a device as claimed in **claim 1**, wherein the semiconducting region comprises organic-inorganic hybrid materials self-assembled from solution (see ¶99, lines 1-2,8-10, Konstantinos et al. is taught by Hirai et al. which actually discloses self-assembly materials, see Konstantinos et al., ¶13, lines 3-6).

4. **Claim 12** is rejected under 35 U.S.C. 102(b) as being anticipated by Choi et al. (Pub No. US 2002/0084459 A1, hereinafter Choi et al.).

FIG. 5



With regards to **claim 1** with dependent **claim 12**, Choi et al. teaches a thin film transistor electronic switching device, comprising:

a source electrode and a drain electrode (see Fig. 5, source electrode **38**, drain electrode **40**);

a semiconducting region in contact with and extending between the source and drain electrodes (see Fig. 5, semiconducting region **44**);

a gate electrode disposed for influencing the transconductance of at least part of the semiconducting region (see Fig. 5, gate electrode **36;** inherent that the gate electrode will influence transconductance since drain current and the gate electrode voltage will change during operation of the device, $g_m = dI / dE$, where dI = change in drain current and dE = change in gate voltage); and

an insulating region located between the source and drain electrodes and configured so that the length of the shortest current path through the semiconducting region between the source and drain electrodes is greater than the shortest physical distance between the source and drain electrodes (see Fig. 5, insulating region **48**,

current path from **38** to **40** shorter than the shortest physical distance between source electrode **38** and drain electrode **40**).

With regards to **claim 12**, Choi et al. teaches a device as claimed in **claim 1**, wherein the semiconductor region is substantially undoped (see ¶69, lines 4-5).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. **Claims 2,17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al. as applied to **claim 1** above.

With regards to **claims 2,17,** Hirai et al. teaches the limitations of **claim 1** for the reasons above.

Hirai et al., however, does not teach shortest current path through the semiconductor region between the source and drain to be greater than 1.05 times the shortest physical distance between the source and drain nor does it teach physical distance between the source and drain to be less than one micrometer.

In the same field of endeavor, given the teaching of the references, it would have been obvious to determine the optimum shortest current path or physical distance between the source and drain electrodes (see *In re Aller, Lacey, and Hall* (10 USPQ 233-237). It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical (se *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ 2d 1934,1936 (Fed. Cir. 1990)).

9. **Claim 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al. as applied to **claim 1** above, and further in view of Han et al. (Pub No. US 2003/0155572 A1, hereinafter Han et al.).

With regards to **claim 15**, Hirai et al. teaches the limitations of **claim 1** for the reasons above.

Hirai et al., however, does not teach an insulating region to comprise of an air gap.

In the same field of endeavor, Han et al. teaches how incorporating air gaps will reduce heat transmission along a vertical direction because it has low thermal conductivity (see ¶24, lines 11-12,16-17).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to include an air gap as taught by Han et al. in order to reduce heat transmission along a vertical direction because it has low thermal conductivity.

10. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al. as applied to **claim 18** above.

With regards to **claim 21**, Hirai et al. teaches the limitations of **claim 18** for the reasons above.

Hirai et al., however, does not teach the thickness of the insulating region to be in the rage of 30 to 80 nm.

In the same field of endeavor, given the teaching of the references, it would have been obvious to determine the optimum thickness of the insulating region (see *In re Aller, Lacey, and Hall* (10 USPQ 233-237). It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical (se *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ 2d 1934,1936 (Fed. Cir. 1990)).

11. **Claim 25** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al. as applied to **claim 18** above, and further in view of Berger et al. ("Projection electron-beam lithography: A new approach, S.D. Berger, J.M. Gibson, R.M. Camarda, hereinafter Berger et al.).

With regards to **claim 25**, Hirai et al. teaches the limitations of **claim 18** for the reasons above.

Hirai et al., however, does not teach forming one or more components of the device using electron beam lithography.

In the same field of endeavor, Berger et al. teaches how electron beam lithography offers high resolution, high throughput, and good overlay and registration characteristics (see Abstract, lines 1-3).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to utilize electron-beam lithography to form one ore more components of the device since electron-beam lithography offers high resolution, high throughput, and good overlay and registration characteristics.

12. **Claim 27** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al. as applied to **claim 18** above, and further in view of David Grewell, Abbass Mokhtarzadeh, Avraham Benatar ("Feasability of Selected Methods for Embossing Micro-features in Thermoplastics", ANTEC 2003, May 4-8, 2003, hereinafter Grewell et al.).

With regards to **claim 27**, Hirai et al. teaches the limitations of **claim 18** for the reasons above.

Hirai et al., however, does not teach using embossing techniques to forming the insulating region.

In the same field of endeavor, Grewell et al. teaches how embossing techniques are utilized since they have the capability to produce features 10 micrometers in width or even in sub-micron range (see Introduction, lines 1-9).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use embossing techniques to forming the insulation region because embossing techniques have the capability to produce features in the sub-micron range as taught by Grewell et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae Lee whose telephone number is 571-270-1224. The examiner can normally be reached on Monday - Friday, 7:30 a.m. - 5:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JML